Notice of References Cited	Application/Control No. 10/064,036	Applicant(s)/Patent Under Reexamination CHUNG ET AL.	
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U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
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FOREIGN PATENT DOCUMENTS

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	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	S.S. Chung et al., "A Novel and Direct Determination of the Interface Traps in Sub-100nm CMOS Devices with Direct Tunnelin Regime (12~16A) Gate Oxide," 2002 Symposium On VLSI Technology Digest of Technical Papers, pages 74-75.
	V	
	W	
	X	

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